REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-23 in the application. In a previous response, the Applicant amended Claims 4, 12 and 20 to correct informalities. In the present response, no claims have been amended, canceled or added. Accordingly, Claims 1-23 are currently pending in the application.

I.   Rejection of Claims 1-23 under 35 U.S.C. §102

The Examiner has rejected Claims 1-23 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,832,292 to Nguyen, *et al.* (Nguyen). The Applicant respectfully disagrees since Nguyen does not teach reducing pipeline stalls between nested calls including storing return PC values in return PC storage located in an execution core of a processor and making ones of the return PC values available to a PC of the processor upon execution of corresponding return instructions as recited in independent Claims 1, 9 and 17.

Nguyen teaches a microprocessor having an Instruction Execution Unit (IEU) 104 and an Instruction Fetch Unit (IFU) 102 that includes a Program Counter (PC) logic unit 270. (*See* column 6, lines 60-63, column 8, lines 42-43, column 12, lines 38-41, and Figures 1-3.) The PC logic unit 270 includes a prefetch PC control unit 364 and an execution PC control unit 366 that provides an address for prefetching. (*See* column 16, lines 43-46, column 17, lines 14-16 and Figure 3.) The prefetch address provides a return address for subsequent use by the prefetch PC control unit 364 when an initial call, trap or procedural instruction occurs. The prefetch address is stored in registers in the prefetch PC control unit 364 upon each occurrence of these instructions. (*See* column 17, lines 16-19.)

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Nguyen does not teach, however, making the prefetch addresses available upon execution of corresponding return instructions. On the contrary, Nguyen teaches selecting one of the return address registers in the prefetch PC control unit 364 to provide a new prefetch virtual address after receiving a return signal. (*See* column 17, lines 21-26.) Thus, instead of making ones of the prefetch addresses available, Nguyen teaches selecting one of the registers after receiving a return instruction. Nguyen, therefore, does not teach making ones of the return PC values available to a PC upon execution of corresponding return instructions as recited in independent Claims 1, 9 and 17.

Thus, the cited reference Nguyen does not teach each and every element of independent Claims 1, 9 and 17 and Claims dependent thereon. Nguyen, therefore does not anticipate Claims 1-23. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 1-23 and allow issuance.

Furthermore, regarding dependent Claims 5, 13 and 21, Nguyen does not teach moving return PC values through registers of a return PC storage as corresponding ones of the return instructions move through stages in a pipeline. Instead, Nguyen stores prefetch addresses in registers of the PC control unit 364 and then selects the appropriate register to obtain a prefetch address after receiving a return signal. (*See* column 17, lines 21-26.) Nguyen does not teach the prefetch addresses move to different registers. Nguyen, therefore, teaches storing prefetch addresses in a designated location and retrieving the prefetch addresses from the designated location instead of moving return PC values through registers of a return PC storage as corresponding ones of the return instructions move through stages in a pipeline as recited in dependent Claims 5, 13 and 21.
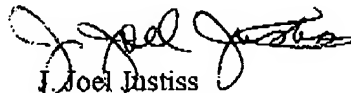
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II.   Conclusion

In view of the foregoing remarks, the Applicant now sees all of the Claims currently

pending in this application to be in condition for allowance and therefore earnestly solicits a Notice

of Allowance for Claims 1-23.

The Applicant requests the Examiner to telephone the undersigned attorney of record at

(972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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